SEMICONDUCTOR STRUCTURE HAVING A COMPENSATED RESISTANCE IN THE LDD AREA AND METHOD FOR PRODUCING THE SAME

BACKGROUND OF THE INVENTION

Cross-Reference to Related Applications:

This application is a continuation of co-pending International Application No. PCT/EP02/09702, filed August 30, 2002, which designated the United States and was not published in English.

1. Field of the invention:

The present invention relates to a semiconductor structure having a compensated resistance in an LDD area and to a method for producing the same, in particular to a semiconductor structure having a compensated resistance in an LDD area. The present invention relates in particular to MOS transistors (MOS = metal oxide semiconductor) wherein between a source area and a drain area a lightly doped drain area is provided which is referred to as an LDD area (LDD = lightly doped drain). In particular, the present invention relates to LDMOS transistors and the production of the same (LDMOS = lateral diffused MOS).

2. Description of the related art:

In MOS transistors for high power applications or in LDMOS transistors for high-frequency power applications between the gate structure and the drain area the LDD area is generated, e.g. by an implantation. In LDMOS transistors before the generation of the source area on the source side of the gate the required channel implantation is

introduced which is then diffused under the gate structure in a subsequent temperature step.

Preferably, in LDMOS transistors for high frequency power applications, on the side of the gate structure facing the drain area, a longer n-doped LDD area is implanted. There are continuous trials to improve the performance of such an LDMOS transistor. An improvement of the performance is for example achieved by an increase of the breakdown voltage or by an improvement of the high frequency characteristics, for example by shielding the gate structure against the drain area. In order to achieve this, the prior art proposes to implant a flat buried area having a p-doping in the n-doped LDD area. This is for example described by H. Söderbärg et al. in "Integration of a Novel High-Voltage Giga-Hertz DMOS Transistor into a Standard CMOS Process", IEEE IEDM Washington 1995, pp. 975-978 and by E. Gebara et al. in "Output Power Characteristics of High Voltage LDMOS Transistors", GHz 2000 Symp. 5th Symp. on Giga-Hertz-Electronics, Proc., Göteborg, p. 13, 14th March 2000, pp. 78-78.

The disadvantage of the preceding methods is that by implantation of the p-region the resistance of the LDD area is increased which is compensated by a correspondingly suitable increase of the doping of the LDD area and by introducing an additional n-doping in the LDD area in the area of the p-region.

In the prior art, a deep LDD area is used which additionally reaches far below the gate structure. The deep LDD area results in the fact that the additionally introduced doping in the p-region only represents a relatively low counter doping to the n-doping of the LDD

area, so that the resistance of the LDD area in the area of the p-region only slightly increases. Further, above the p-region an additional n-doping is introduced, so that the p-region is completely buried in the LDD area.

It is a disadvantage of the deep LDD area that the same reaches far below the gate structure which leads to an increase of the drain-gate-capacity which is in particular undesirable in the RF area. However, this deep LDD area which therefore reaches below the gate structure may not be omitted in order to guarantee the shielding of the gate structure with a simultaneous compensation of the resistance increase due to the p-region. Suggestions for a compensation of the resistance increase in comparatively flat LDD areas which do not reach below the gate structure and therefore comprise a low gate-drain-capacity are not known in the prior art.

SUMMARY OF THE INVENTION

It is the object of the present invention to provide an improved semiconductor structure and a method for producing the same, whereby a semiconductor structure is obtained comprising improved characteristics, in particular in the RF area.

According to a first aspect, the present invention provides a semiconductor structure having a substrate, a source area formed in the substrate and a drain area also formed in the substrate. The drain area has a doping of a first conductivity type and includes a first drain portion with a first doping concentration and a second drain portion with a second doping concentration. The first doping concentration is higher than the second doping

concentration. Further, in the second drain portion a first region is formed comprising a doping of a second conductivity type which is different from the first conductivity type. The semiconductor structure further includes a second region formed in the structure below the second drain portion and comprising a doping of the first conductivity type. Further, between the source area and the second drain portion a channel area is established in the substrate.

According to a second aspect, the present invention further provides a method for producing a semiconductor structure in which first a gate structure on a substrate is generated, a source area with a doping of a first conductivity type in the substrate is generated and a drain area with a doping of the first conductivity type in the substrate is generated. The drain area is generated by forming a first drain portion with a first doping concentration and a second drain portion with a second doping concentration which is lower than the first doping concentration, wherein the second drain portion is formed between the first drain portion and the gate structure. Further, a first region in the second drain portion is generated by introducing a doping of a second conductivity type into the second drain portion, and a second region is generated below the drain portion in the substrate by introducing a doping of the first conductivity type.

According to the present invention, a semiconductor structure is provided in which the LDD area substantially does not extend below the gate structure, so that a high gate-drain-capacity is prevented.

This is preferably achieved by the fact that the generation of the LDD area, e.g. by implantation, is only performed after the gate structuring. Instead of the initial structuring of the gate structure also a corresponding masking may be provided, so that an implantation in this case may be performed before the gate structuring. Further, other measures known in the prior art may be used in order to guarantee that an LDD area basically only abuts on the gate structure, however, does not reach below the gate structure.

The generation of the LDD area, e.g by implantation, after the gate structuring leads to a flat LDD area, so that the additional p-region also needs to be flat for improving the characteristics of the LDMOS transistor. As a result of this, the resistance of the LDD area in the area of the p-region strongly increases. In order to compensate for this increase, an additional n-region is required which is preferably generated using the same mask as the p-region. In contrast to the prior art, the additional n-region is generated below the LDD area in the substrate, e.g. by implantation, so that the LDD area is extended to the bottom (in the direction of the substrate) in these areas.

According to one embodiment, the p-region of the LDD area remains floating, i.e. is not connected to a potential. According to another embodiment, the p-region is connected to a reference potential, e.g. mask, whereby a defined charge carrier degradation is achieved.

It is the advantage of the present invention that in the area of the gate structure a flat LDD area is generated which does not extended below the gate structure, so that the gate-drain-capacity is held low.

In contrast to the methods known in the prior art, here in addition to the initial LDD area an additional n-region is introduced below the original LDD area in order to compensate for the resistance increase of the LDD area in the area of the p-region. In contrast to the prior art, the p-doping of the p-region in the flat LDD area represents a substantial counter-doping which is compensated by the inventive approach. In contrast to the prior art, the additional n-region is arranged below the p-region and below the LDD area, i.e. in the substrate. Whereby, compared to the prior art, a comparatively flat LDD area is enabled.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become clear from the following description taken in conjunction with the accompanying drawings, in which:

Fig. 1 shows an illustration of an LDMOS transistor having a dual implanted LDD area according to the present invention;

Fig. 2 shows a graph representing the input characteristic line of the LDMOS transistor of Fig. 1 for different implantations in the LDD area; and

Fig. 3 shows a graph representing the breakdown characteristic line of the LDMOS transistor of Fig. 1 for different implantations in the LDD area.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In Fig. 1 an LDMOS transistor with a p/n-dual implantation in the LDD area is illustrated according to the present invention. The LDMOS transistor is formed in a substrate 100 which is for example a p-substrate. In Fig. 1, only the substrate 100 is illustrated, however, according to the present invention, the term "substrate" also relates to a structure including a substrate layer and an epitaxy layer on the substrate layer.

The substrate 100 has a p-doping of about 3×10^{15} $1/cm^3$. On a surface 102 of the substrate 100 a gate structure 104 is formed including a gate polysilicon 106 and a gate oxide 108 arranged between the gate polysilicon 106 and the substrate 100. Within the substrate 100 further an n^+-source area 110 and an n^+-drain area 112 are formed. Below the gate oxide 108 a laterally diffused channel area 114 is formed comprising a p-doping in the area of about 2×10^{17} $1/cm^3$. The source area 110 and the drain area 112 respectively comprise n-dopings of about 2×10^{20} $1/cm^3$.

Between the gate structure 104 and the drain area 112 an LDD area 116 is formed e.g. by implantation comprising a doping concentration which is lower than the doping concentration of the drain area. In the illustrated embodiment, the doping concentration of the LDD area is at about 1×10^{17} $1/cm^3$.

For improving the performance of the LDMOS transistor, a p-region 118 is formed in the LDD area 116, e.g. by implantation, having a p-doping dose of approx. 1×10^{12} $1/cm^2$.

In order to prevent a resistance increase due to the introduced flat p-region 118 in the LDD area 116 of the LDMOS transistor, a further n-region 120 is provided lying below the p-region 118 and below the LDD area, i.e. in the substrate. The doping of the further n-region 120 is preferably performed with a dose of about 2×10^{12} $1/cm^2$.

At 122 in Fig. 1 the area of the dual implantation in the LDMOS transistor is exemplified.

In the embodiment illustrated in Fig. 1, the implantation of the LDD area 116 was performed before the deposition of the polymaterial of the gate structure 106. The LDD area 116 is generated by implantation of arsenic (As) at 80 keV with a dose of about 1.3×10^{12} $1/cm^2$. The p-region 118 is generated by implantation of boron (B) at 18 keV with a dose of about 1×10^{12} $1/cm^2$. Both implantations are performed at an angle of 0° with regard to the normal on the substrate surface 102.

The further n-region 120 is generated by an implantation of phosphorus (P) at 300 keV with a dose of about 2×10^{12} $1/cm^2$. The implantation was performed at an angle of 7° with regard to the normal on the substrate surface 102 and the substrate (wafer disc) was rotated four times during the implantation ("quad mode"), in order to thus guarantee a uniform generation of the implantation of the n-region 120.

During production the implantation of the n-region 120 is performed using the same mask which was used for the implantation of the p-region. This leads to the defined area 122 shown in Fig. 1.

In one alternative embodiment, the LDD area 116 may be generated by an implantation of phosphorus (P) at 100 keV with a dose of about 1.2×10^{12} $1/cm^2$.

Although in Fig. 1 the p-region 118 is shown exposed at the surface 102 of the substrate, the p-region may also be completely embedded in the LDD area 116.

According to one embodiment of the present invention, the p-region 118 is connected to no reference potential, i.e. is "floating". In another embodiment, the p-region 118 may be connected to a reference potential, e.g. to ground, whereby a defined charge decomposition may be achieved.

With reference to Fig. 2, the improvement of the input characteristic line is illustrated by the inventive dual implantation in the flat LDD area 116. In Fig. 2, the gate voltage is plotted versus the drain current, wherein four curves 1 to 4 are shown. The curves shown in Fig. 2 were determined for a drain voltage of 26 Volt and show the dependence of the drain current on the applied gate voltage.

Curve 1 shows the course of the input characteristic line after only the LDD area 116 has been implanted.

Fig. 2 shows the course of the input characteristic line after the additional p-region 118 was implanted into the LDD area 116. As may be seen, the characteristic line is lowered, due to the p-region 118 increasing the resistance in the LDD area 116 so that the drain current correspondingly decreases compared to the LDD area without an additional p-region 118 (curve 1).

Curve 3 shows a simulation in which in addition to the LDD-area 116 only the further n-region 120 was introduced below the LDD area.

Curve 4 indicates the course of the input characteristic line, as it is obtained for an LDMOS transistor according to Fig. 1, wherein in the LDD area 116 the p-region 118 is implanted and the n-region 120 is introduced below the LDD area 116. As it may be seen, despite the additional p-region 118 in the LDD area 116 (which invariably leads to an increase of the resistance (see curve 2)) the presence of the further n-region 120 prevents the undesired resistance increase. Even an improvement of the input characteristic line (curve 4) compared to the LDD area is achieved without additional n-implantation (curve 1).

It is therefore to be noted that by the inventive approach of providing an additional n-region 120 below the LDD area, the resistance increase due to the p-region 118 may be prevented. The presence of this additional n-region 120 permits the advantageous effects of the p-region 118 in the LDD area 116, i.e. the shielding of the gate structure to be recognized without disadvantageous limitations of the characteristics of the RF transistor.

Fig. 3 is a graphical illustration of the breakdown characteristic line wherein the drain current is plotted versus the drain voltage.

Just like in Fig. 2, curve 1 designates the course of the breakdown characteristic line in an LDMOS transistor which only comprises the LDD area 116.

Curve 2 shows the course of the breakdown characteristic line of an LDMOS transistor with an LDD area 116 in which a p-region 118 was implanted.

For comparative purposes, curve 3 shows the course of the breakdown characteristic line for an LDD area 116 below which a further n-region 120 was introduced.

Curve 4 shows the course of the breakdown characteristic line of an LDMOS transistor wherein the p-region 118 is introduced in the LDD area 116 and below the LDD area 116 the further n-region 120 is introduced.

As it may be seen from a comparison of curves 1 and 2, by the introduction of the p-region 118 into the LDD area 116 the breakdown voltage is substantially reduced, from about 76 Volt to about 67 Volt. This reduction of the breakdown voltage may be compensated and even improved by the additional n-region 120 below the LDD area 116, as is illustrated by curve 4, in which the breakdown voltage may be increased to about 79 Volts.

With regard to Figs. 2 and 3 it is to be noted that here an LDMOS transistor according to Fig. 1 was assumed, in which the LDD area 116 was generated by an implantation of arsenic (As) at about 80 keV with a dose of 1.3×10^{12} $1/cm^2$, wherein the implantation is performed before the deposition of the gate polysilicon 106. The p-region 118 was generated by an implantation of boron (B) at about 18 keV with a dose of about 1×10^{12} $1/cm^2$. The further n-region was generated by an implantation of phosphorus (P) at about 300 keV with a dose of about 2×10^{12} $1/cm^2$. The implantation is performed at an angle of about 7° with regard to the normal on the surface 102, wherein the disc

was rotated four times according to the so called "quad mode".

Although the above description of the preferred embodiments of the present invention was performed using an LDMOS transistor having an LDD area, it is noted, that the inventive method may also be applied for MOS transistors comprising an LDD area.

The present invention is not restricted to the above-described materials. Instead of the illustrated p-substrate 100, p-region 118, n-source area 110, n-drain area 112, n-LDD area 116 and a further n-region 120 complementary materials may be used, i.e. an n-substrate 100, an n-area 118; a p-source area 110, a p-drain area 112, a p-LDD area 116 and a further p-region 120 may be used to form a semiconductor.

Further, the invention is not restricted to the implantation of the above-mentioned materials for the generation of the respective areas in the substrate. Other known technologies may also be used.

While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents which fall in the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and compositions of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall in the true spirit and scope of the present invention.